

**LISTING OF THE CLAIMS:**

Claims 1-8 (cancelled).

9. (Currently Amended) A method for producing an integrated semiconductor component comprising the steps of preparing a semiconductor substrate having at least one first region and at least one second region; producing gate paths in the first region and the second region of the semiconductor substrate; producing source/drain regions neighboring the gate paths in the first region of the semiconductor substrate; forming ~~at least two~~ spacers on gate paths in the first region; producing source/drain regions neighboring the gate paths in the second region of the semiconductor substrate; forming sacrificial contacts in the second region ~~before all ; then forming additional spacers are formed in the first region; removing a portion of the sacrificial contacts to expose source/drain regions in the second region~~ and preparing contacts to predetermined source/drain regions in the second region and the first region.

10. (Previously Presented) A method according to claim 9, wherein the spacers are formed of a material selected from a group consisting of silicon oxide, silicon nitride and oxynitride.

11. (Previously Presented) A method according to claim 9, wherein the step of producing gate paths includes applying a polysilicon layer on the semiconductor substrate, providing a protective layer selected from a group consisting of silicon nitride, silicon oxide and oxynitride layers on the polysilicon layer and then structuring the polysilicon layer and protective layer to form the gate path.

12. (Previously Presented) A method according to claim 11, wherein the protective layer is formed with a thickness so that the protective layer exhibits a thickness of less than 100nm after the structuring step.

13. (Currently Amended) A method according to claim 11, which includes, after the step of forming sacrificial contacts and prior to the step of preparing contacts to the predetermined source/drain regions, removing the protective layer from the gate paths, at

least in the first region, and then doping the gate paths in the first region with ~~a-dopant dopants~~ having different conductive types.--

14. (Previously Presented) A method according to claim 13, which includes, after the step of doping the gate paths in the first region, generating a silicide layer on the doped gate paths of the first region of the semiconductor substrate.

15. (Previously Presented) A method according to claim 14, wherein the silicide layer is selected from silicides consisting of  $\text{CoSi}_2$ ,  $\text{TaSi}_2$ ,  $\text{TiSi}_2$  and  $\text{WSi}_x$ .

16. (Previously Presented) A method according to claim 15, wherein the step of generating a silicide comprises the step of providing a metal selected from Co, Ta, Ti and W on the gate paths of the first region and subsequently heating to convert the metal into a metal silicide layer.

17. (Previously Presented) A method according to claim 14, wherein the step of generating a silicide layer on the gate paths of the first region includes applying a metal capable of forming a silicide onto the gate paths of the first region and subsequently heating to create the silicide layer.

18. (Previously Presented) A method according to claim 9, which includes, prior to the step of forming contacts to the predetermined source/drain region of the second region, generating silicide layers on the gate paths of the first region of the semiconductor substrate.--